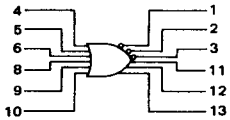
MC1001 thru MC1003
MC1201 thru MC1203

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

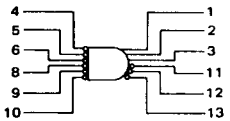
POSITIVE LOGIC



$1 = \overline{4 + 5 + 6 + 8 + 9 + 10}$

$11 = 4 + 5 + 6 + 8 + 9 + 10$

NEGATIVE LOGIC



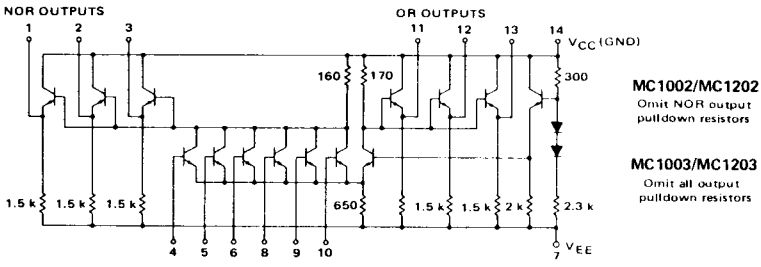
$1 = \overline{4 \cdot 5 \cdot 6 \cdot 8 \cdot 9 \cdot 10}$

$11 = 4 \cdot 5 \cdot 6 \cdot 8 \cdot 9 \cdot 10$

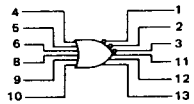
DC Input Loading Factor = 2
DC Output Loading Factor = 25

Power Dissipation = MC1001/MC1201 – 115 mW typical
MC1002/MC1202 – 80 mW typical
MC1003/MC1203 – 40 mW typical

MC1001/MC1201 CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1201-1203 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1001-1003 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7														
MC1201/MC1001			-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc
MC1202/MC1002			-	-	-	22	-	-		-	-	-	22	-	-	
MC1203/MC1003			-	-	-	11	-	-		-	-	-	11	-	-	
Input Current	I_{in}	4	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
		5	-	-	-		-	-		-	-	-		-	-	
		6	-	-	-		-	-		-	-	-		-	-	
		8	-	-	-		-	-		-	-	-		-	-	
		9	-	-	-		-	-		-	-	-		-	-	
		10	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage	V_{OH}‡	1, 2, 3†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	1, 2, 3†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	11, 12, 13†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	11, 12, 13†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{4+1-}	1	4.0	7.5	4.0	7.0	6.0	9.0	ns	4.0	7.0	4.0	7.0	5.0	8.0	ns
	t_{4-1+}	1					6.0	9.0								
	t_{4+11+}	11					5.0	9.0								
	t_{4-11-}	11					6.0	9.0								
(Fan-Out = 15)	t_{4+1-}	1	18	-	18	-	22	-		18	-	18	-	20	-	
	t_{4-1+}	1	6.0	-	6.0	-	8.0	-		6.0	-	6.0	-	7.0	-	
	t_{4+11+}	11	4.0	-	4.0	-	6.0	-		4.0	-	4.0	-	5.0	-	
	t_{4-11-}	11	13	-	13	-	17	-		13	-	13	-	15	-	
Rise Time (Fan-Out = 3)	t_{1+}	1	5.0	8.0	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.5	8.0	
	t_{11+}	11	4.0	7.0	4.0	6.5	5.0	8.0		4.0	6.5	4.0	6.5	4.5	7.0	
Fall Time (Fan-Out = 3)	t_{1-}	1	6.0	8.5	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.5	9.0	
	t_{11-}	11	6.0	8.0	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.5	9.0	

* Individually test each input using the pin connections shown.
† Individually test each output listed using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.

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@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	mAdc I_L
MC1201-1203	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1001-1003	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current MC1201/MC1001 MC1202/MC1002 MC1203/MC1003	I_E	7	-	-	-	4,5,6,7,8,9,10	-	14
Input Current	I_{in}	4	-	-	4	5,6,7,8,9,10	-	14
		5	-	-	5	4,6,7,8,9,10	-	
		6	-	-	6	4,5,7,8,9,10	-	
		8	-	-	8	4,5,6,7,9,10	-	
		9	-	-	9	4,5,6,7,8,10	-	
		10	-	-	10	4,5,6,7,8,9	-	
Input Leakage Current	I_R	Inputs*	-	-	-	4,5,6,7,8,9,10	-	14
"NOR" Logical "1" Output Voltage	V_{OH}‡	1, 2, 3†	4	-	-	5,6,7,8,9,10	1	14
			5	-	-	4,6,7,8,9,10		
			6	-	-	4,5,7,8,9,10		
			8	-	-	4,5,6,7,9,10		
			9	-	-	4,5,6,7,8,10		
			10	-	-	4,5,6,7,8,9		
"NOR" Logical "0" Output Voltage	V_{OL}	1, 2, 3†	-	4	-	5,6,7,8,9,10	-	14
			-	5	-	4,6,7,8,9,10	-	
			-	6	-	4,5,7,8,9,10	-	
			-	8	-	4,5,6,7,9,10	-	
			-	9	-	4,5,6,7,8,10	-	
			-	10	-	4,5,6,7,8,9	-	
"OR" Logical "1" Output Voltage‡	V_{OH}‡	11, 12, 13†	-	4	-	5,6,7,8,9,10	1	14
			-	5	-	4,6,7,8,9,10		
			-	6	-	4,5,7,8,9,10		
			-	8	-	4,5,6,7,9,10		
			-	9	-	4,5,6,7,8,10		
			-	10	-	4,5,6,7,8,9		
"OR" Logical "0" Output Voltage	V_{OL}	11, 12, 13†	4	-	-	5,6,7,8,9,10	-	14
			5	-	-	4,6,7,8,9,10	-	
			6	-	-	4,5,7,8,9,10	-	
			8	-	-	4,5,6,7,9,10	-	
			9	-	-	4,5,6,7,8,10	-	
			10	-	-	4,5,6,7,8,9	-	
Switching Times Propagation Delay			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
(Fan-Out = 3)	t_{4+1-}	1	4	1	-	5,6,7,8,9,10	-	14
	t_{4-1+}	1		1	-		-	
	t_{4+11+}	11		11	-		-	
	t_{4-11-}	11		11	-		-	
(Fan-Out = 15)	t_{4+1-}	1		1	-		-	
	t_{4-1+}	1		1	-		-	
	t_{4+11+}	11		11	-		-	
	t_{4-11-}	11		11	-		-	
Rise Time (Fan-Out = 3)	t_{1+}	1		1	-		-	
	t_{11+}	11		11	-		-	
Fall Time (Fan-Out = 3)	t_{1-}	1		1	-		-	
	t_{11-}	11		11	-		-	

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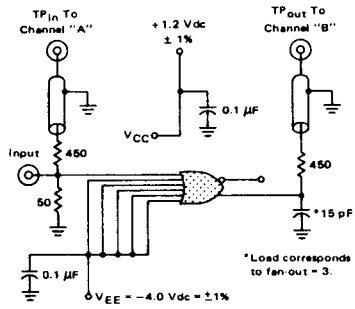
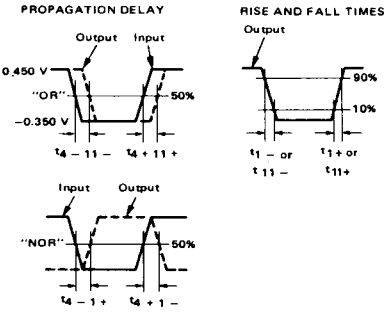
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input pulse t_r and t_f = 5.0 ± 0.5 ns



Switching waveforms shown for pulse in on pin 4 and pulse out on pins 1 and 11, however all other input-output combinations will meet the limits specified.

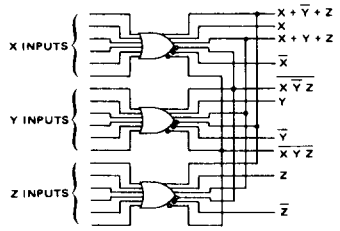
APPLICATIONS INFORMATION

The MC1001-1003/MC1201-1203 6-input OR/NOR gates are extremely useful in generating multiple wired-OR logic functions since six independent outputs are provided. (An example is shown in Figure 1.) The gate performs well as a clock driver with the multiple outputs which result in three times the normal fan-out for a given clock waveform. If twisted pair lines are being used for clock distribution in a system, the gate will drive three independent twisted pair lines, each with the same clock waveform.

An output impedance of about 2 ohms is obtained if three OR or NOR outputs are tied together. This provides an excellent 50-ohm driving capability. The 50-ohm line or coax should be terminated in its characteristic impedance to a nominal −2.0 V. This prevents excessively high output current that would pull the logic "1" level below nominal (see Figure 2).

FIGURE 1 - MECL II "WIRED OR" FEATURE

EXAMPLE SHOWN FOR ONE POSSIBLE COMBINATION OF OUTPUTS



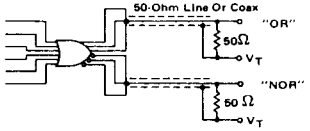
WHERE:
X = f (Six Variables)
Y = f (Six Variables)
Z = f (Six Variables)

t_{pd} Average = 4.0 ns
Total Power = 200 mW

NOTE:
All Outputs That Are Used Require An Internal or External Pulldown Resistor.

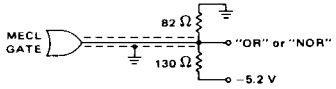
FIGURE 2 - MC1003/MC1203 AS A 50-OHM DRIVER WITH NOMINAL MECL LOGIC LEVELS

50-OHM TERMINATION TO SEPARATE NEGATIVE VOLTAGE



$V_T \approx -2.0$ V Well Bypassed To Ground

50 OHM TERMINATION TO MECL POWER SUPPLY



Output Logic Swing ≈ 0.8 V
Typical Gate Propagation Delay = 4.0 ns
Typical Rise Time At 50-Ohm Load = 7.0 ns
Typical Fall Time At 50-Ohm Load = 7.0 ns

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